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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHEW, JOHN	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/624,816	VOGEL ET AL.	
	Examiner	Art Unit	
	John L Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 07282004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 39-44 is/are allowed.

6)☒ Claim(s) 1-6,10,11,24-26,32-34,36,38,45 and 46 is/are rejected.

7)☒ Claim(s) 7-9, 12-23, 27-31, 35, 37 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 24, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Jain et al.

Claim 1, 24 Jain teaches a protocol for devices (column 1 lines 7-13) referenced by a data link protocol, comprising a serial bus (column 1 lines 18-22) referenced by a data transmission in serial fashion, for communication between a pair of devices (Fig. 1) referenced by computer A and computer B, utilizing a protocol comprising a plurality of digital bits (column 2 lines 15-18) referenced by unique pattern of ones and zeros, in a predetermined format (column 1 lines 7-13) referenced by HDLC of ISO Standard 3309, comprising a frame forming a framing cycle and a data cycle (column 2 lines 3-6, lines 19-23) referenced by the HDLC control symbol and data stream, said devices formatting digital bits in predetermined frame format (Fig. 2) referenced by flowchart of transmitter algorithm, having no requirement for DC balance (column 1 lines 60-68, column 2 lines

1-2) referenced by asymmetrical DC unbalanced run-length codes. The DC unbalanced code inherently has an absence of DC balance in their voltage levels. Jain teaches by incorporation of the prior art HDLC specification, a framing cycle carrying information relating to the protocol referenced by HDLC address bits, data cycle carrying informational data referenced by HDLC data bits, protocol characterized by voltage levels of bits on frame cycles having no DC balance (column 1 lines 60-62, column 2 lines 1-2) referenced by asymmetrical run length codes being DC unbalanced, which inherently implies a DC voltage level and no requirement of balance of bits.

Claim 32, Jain teaches a method of transmitting data according to a protocol (column 1 lines 7-13) referenced by ISO standard 3309 for HDLC, comprising the steps of forming a packet of data comprising digital bits (Fig. 2) referenced by the transmission of frame delimiter step 42, having a HIGH and LOW voltage (column 2 lines 1-2) referenced by the HDLC being an asymmetric run-length code being DC unbalanced which implies DC voltage for a high/low state, parsing said packet of data into a plurality of frames (Fig. 4) referenced by receiver flowchart to parse for delimiter, parsing each frame into a plurality of bits for a data cycle and a frame cycle (column 2 lines 15-21) referenced by the delimiter for the frame cycle and the containment of data within the frame, transmitting the plurality of frames (Fig. 2) referenced by the transmitter flowchart with step 42 sending the delimiter, wherein the bits of data cycles and frame cycles are characterized by an absence of DC balance in their hi/low voltages (column 1 lines 60-

62, column 2 lines 1-2) referenced by the HDLC being asymmetrical and is DC unbalanced which inherently implies an absence of DC balance in the voltage.

Claim 33, Jain teaches connecting two devices with a bus that transmits data serially (Fig. 1, column 1 lines 18-22) referenced by transmitter 18 and receiver 20 with data transmission in a serial fashion

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 4, 10, 25, 26, 34, 36 and 45, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al. as applied to claims 1, 24, 32 and 33 above, and in view of Bastiani et al.

Claim 2, Jain teaches a pair of devices comprising a transmitting circuit and a receiving circuit (Fig. 1) referenced by transmitter 18 and receiver 20, communicating serially with

one another on said bus (Fig. 1) referenced by communication path 12, with plurality of digital bits having HIGH and LOW voltage levels (Fig. 1, column 6 lines 25-28) referenced by digital transmitter circuitry which inherently has high/low voltage levels, wherein packet bits are characterized by absence of DC balance in average voltage levels (column 1 lines 60-68, column 2 lines 1-2) referenced by asymmetrical DC unbalanced run-length codes which have no DC balance in average voltage levels. Jain does not teach a transmitting circuit and receiving circuit being in substantially close proximity.

Bastiani teaches transmitting circuit and receiving circuit being in substantially close proximity to one another (FIG. 12) referenced by the transceivers separation of 1.5 meter max.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the frame delimiter protocol taught by Jain in conjunction with the communication protocol of Bastiani for the purpose of a more robust protocol that can improve communication performance.

Claims 3, 4, 10, 25, 26, 34, 36 and 45, Jain teaches a protocol for devices (column 1 lines 7-13) referenced by a data link protocol, comprising a serial bus (column 1 lines 18-22) referenced by data transmission in serial fashion, for communication between a pair of devices (Fig. 1) referenced by computer A and computer B, utilizing a protocol comprising a plurality of digital bits (column 2 lines 15-18) referenced by unique pattern

of ones and zeros, having no requirement for DC balance (column 1 lines 60-68, column 2 lines 1-2) referenced by asymmetrical DC unbalanced run-length codes. The DC unbalanced code inherently has an absence of DC balance in their voltage levels. Jain teaches a frame cycle comprising bits delimiting a frame (column 2 lines 7-9, column 2 lines 15-18) referenced by the delimiting pattern 01111110.

Jain does not teach transmitting and receiving circuits sharing the same ground, nor a framing cycle with a first control information and a leftover framing bits for carrying a second control information, nor leftover control bits used for error correction, nor fabrication of electronic circuits in close proximity and sharing a common ground.

By incorporating the HDLC delimiter of Jain with the protocol of Bastiani wherein the HDLC delimiter of Jain substitutes for the SYNC field of Bastiani (FIG. 20), Bastiani teaches a protocol transmission of a plurality of digital bits (FIG. 16) in a predetermined format (FIG. 20), the predetermined format comprising a frame cycle represented by the SYNC, PT, BC and DT frames and a data cycle represented by DATA frame. Bastiani teaches voltage levels associated with the digital bits (TABLE 18) referenced by V_{oh} and V_{ol}. Bastiani teaches a transmitting and receiving circuit (FIG. 12) referenced by transceivers 202a and 202b, communicating serially referenced by TP 204, having voltage levels of HIGH and LOW (TABLE 18) referenced by V_{oh} at 1475mV and V_{ol} at 925mV, transmitting and receiving circuit in substantially close proximity to each other (FIG. 12) referenced by 1.5 meter max.

Claim 3, Bastiani teaches a transmitting and receiving circuits sharing the same ground (column 16 lines 9-16) referenced by a twisted pair used for grounds.

Claims 4, 25, 36, 45 Bastiani teaches a framing cycle comprising a predetermined number of bits for control (FIG. 20) referenced by the SYNC, PT, BC DT fields, with a first predetermined number of bits for first control information referenced by the SYNC field, a second leftover predetermined number of bits for second control information referenced by PT, BC and DT fields.

Claim 10, 26, Bastiani teaches leftover control bits include error correction information (FIG. 20, column 2 lines 31-35) referenced by PT.

Claim 34, Bastiani teaches fabricating devices from electronic circuits (FIG. 14A) referenced by encoding circuit 210, in substantial close proximity (FIG. 12) referenced by 1.5 meter max, sharing a common ground (column 16 lines 9-16) referenced by a twisted pair for grounds.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the frame delimiter protocol taught by Jain in conjunction with the communication protocol of Bastiani for the purpose of a more robust protocol that can improve communication performance.

2. Claims 5 and 6, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain and Bastiani as applied to claims 1-4, 10, 24-26, 32-34 and 36 above, and further in view of Derby et al. Jain and Bastiani teaches an HDLC delimiter with a serial communication protocol. Jain and Bastiani does not teach framing cycle bits that alternate in value between HIGH and LOW between successive frames.

Claims 5 and 38, Derby teaches a frame (FIG. 8) with a synchronization pattern alternating between HIGH and LOW (column 4 lines 63-66). This synchronization pattern can be used in place of the HDLC delimiter taught by Jain in conjunction with the protocol of Bastiani.

Claim 6, Bastiani teaches a framing cycle comprising a predetermined number of bits for control (FIG. 20) referenced by the SYNC, PT, BC DT fields, with a first predetermined number of bits for first control information referenced by the SYNC field, a second leftover predetermined number of bits for second control information referenced by PT, BC and DT fields.

It would have been obvious to one skilled in the art at the time of the invention to use an alternating HIGH and LOW pattern to synchronize a frame. This simplistic pattern

greatly reduces the bandwidth required for synchronization purposes as taught by Derby (column 1 lines 61-67).

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jain and Bastiani as applied to claims 1-4, 10, 24-26, 32-34 and 36 above, and further in view of Bernath. Jain teaches a HDLC delimiter which is incorporated into the protocol of Bastiani. Bastiani teaches error correction bits (FIG. 20) referenced by CRC field. Bastiani teaches the use of a polynomial code for checksum error detection (column 27 lines 65-67, column 28 lines 36-41). Bastiani teaches the use of synchronous communication (column 7 lines 38-41) referenced by the use of data strobe links. Bastiani does not each the location of the error correction CRC field to be part of the leftover control bits, or equivalently the header section. Bernath teaches an error correction field (FIGURE 2) CRC field 204 after the Frame Header 202 which is used for control information (column 7 lines 38-43). This shows the CRC field is effectively part of the header section.

It would have been obvious to one skilled in the art at the time of the invention to place the CRC field with the header section of the protocol taught by Bastiani for the purpose of making the CRC value immediately available for comparison once the calculation is performed.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nickolis et al. in view of Jain et al.

Claim 46, Nickolis teaches a system of devices comprising a backplane (column 7 lines 22-43) referenced by the router connections to the backplane for Processor Element to Processor Element communications, a plurality of serial buses framed within the backplane (FIG. 1) referenced by the plurality of serial buses 22 between the Processor Element Array 20 and the Router Interconnection Network 30, a plurality of said transmitting and receiving circuits coupled to said plurality of serial buses (FIG. 6, column 8 lines 45-67) referenced by an array of drivers/decoders 529 coupled to the bit-serial bus 504, such that one transmitting circuit and one receiving circuit share a respective one of said plurality of serial buses thereby forming a parallel configuration (FIG. 6) referenced by each of the Router I/O channels 500.0-500.63 coupled to a bit-serial bus in a parallel configuration, wherein each pair of said circuits share a same ground (column 18 lines 52-67, column 19 lines 1-25) referenced by the Table 1 embodiment of the RIO chip with a common output ground pin 12 and common internal ground pin 4, reducing bus overhead (FIG. 6) referenced by the reduction of parallel bus lines by serial bus lines between the Processor Element Array and the Router I/O Element Array, and enabling said circuits to perform clock recovery (column 22 lines 62-67, column 23 lines 17-31) referenced by Table 5 SCLK the serial-scan clock.

Nickolis does not teach an improved protocol, synchronously communicating utilizing a protocol that formats into frames, enabling clock recovery nor absence of DC balance. Jain teaches providing an improved protocol (Abstract lines 1-4) referenced by a strong framing method to detect errors, synchronously communicating a plurality of digital bits across said serial buses (column 1 lines 15-22) referenced by the data transmission in a serial fashion, utilizing a protocol that formats said digital bits into frames (column 1 lines 27-34) referenced by the merging of data and control information into a frame for transmission as a bit-oriented data link protocol, wherein each of said frames includes one framing cycle and a plurality of data cycles (Fig. 3, column 2 lines 3-18) referenced by the delimiter for a framing cycle and the transmission of data equated to data cycles between delimiters, said circuits having no requirement for DC balance when formatting said digital bits such that voltage levels of said bits of said frames have an absence of DC balance (column 1 lines 63-67, column 2 lines 1-2) referenced by the run length code being DC unbalanced.

It would have been obvious to one skilled in the art at the time of the invention to use the framing protocol of Jain to the parallel processing system of Nickolis for the purpose improving error detection probability.

Allowable Subject Matter

4. Claims 7-9, 12-23, 27-31, 35 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 39-44 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art search did not disclose the use of serial buses configured in parallel with framing information of the serial bus partitioned into first control information and second control information, with the second control information bits referencing data cycles.

Response to Arguments

On a subsequent prior art search, claim 46 has been rejected per the citation above.

Rejection for claims 1, 24, 32 and 33 are maintained.

Jain teaches that HDLC run length code is asymmetrical and is DC unbalanced. He does not teach DC balance. The claim limitation cites "no requirement for DC balance" or "absence of DC balance" which equates to an unbalanced condition which is taught by Jain. The mechanism is through the creation of the string of bit values which

corresponds to a voltage levels for 0 and 1. This inherently results in a DC average voltage level unless the number of 0's equal the number of 1's and a bipolar voltage levels are used. Therefore unless there is a requirement for DC balance, the inventor would not compensate for such through a DC offset value, so the end result is an unbalanced condition.

Claim 2 is rejected by revised art combination.

Claim 46 is reject by new art combination.
Jain does not teach clock recovery. Jain's disclosure teaches only serial transmission Nickolis teaches serial bus transmission in a parallel structure. The clock recovery is obtained from the serial-scan clock function of the SCLK signal.

Jain disclosure is focused on error detection. It also has elements of data transmission particularly in regards to the protocol used for delimiting and framing which is applicable to this application.

The argument that the combination of Bastiani and Jain fails to teach the features of the invention is not persuasive. The term "frame" is well known and established in the industry. Neither Bastiani nor Jain uses the term "frame" in a manner contrary to the known art. To differentiate the term "frame" in the invention, the claim must be very clear as to the differences to the term "frame" used by Bastiani or Jain.

Jain discloses a more robust HDLC technique. Although it is an upper layer protocol in comparision to the lower physical layer, the features of it's limitations is still applicable. The claims of the applicant's invention does not specify the protocol level at which the data is transmitted.

The rejections for claims 3, 4, 5, 6, 10, 11, 25, 26, 34, 36 and 45 are maintained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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